Stress induced by Silicon-Germanium integration in Field Effect Transistors

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Introduction

Historically, the CMOS performances were increased owing dimensions scaling. However, this approach is no longer efficient and today a solution is to integrate **high level of stress in the devices**. This way, the drain current is enhanced enabling high frequency circuits. High level of stress is obtained through the **integration of Silicon-Germanium**. The lattice mismatch between Si and $Si_{0.75}Ge_{0.25}$ leads to a strain of ε=-0.94% equivalent to a stress of **σ=-1.6GPa** (Figure 1). Two different studies have been addressed with the help of simulations using COMSOL software. The first study aims to quantify the **stress relaxation at the edges** of active area. The second study is related to the additional stress obtained via the **integration of $Si_{1-y}Ge_y$ in Source/Drain regions** and according to different Germanium contents.

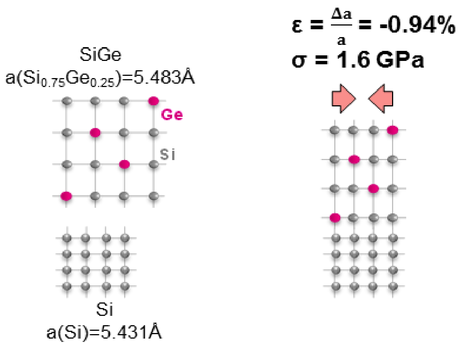

Figure 1: Illustration of initial stress in SiGe alloy induced by lattice mismatch

Computational method

The structural mechanical module has been used in a **static analysis**. SiGe was modelled by a **linear elastic material with initial strain ε** according to the amount of Ge. One has to be careful with the sign of strain ε that has to be defined in “initial stress and strain” feature. To properly model a SiGe material in compression**, whereas the strain is negative (ε=-0.94% for 25% of Ge), the value in “initial stress and strain” feature must be positive**. This strain value must be applied in **all directions** in the same way. The final level of strain in the SiGe film is determined through boundary conditions.

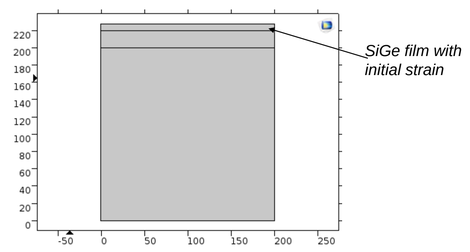

Figure 2: Simple 2D geometry used in study 1 with SiGe film as top layer (left). Initial stress and strain values for the SiGe film to consider lattice mismatch with eps0 postivie value for compressive strain (right).

1. Relaxation on active edges

After SiGe integration, the film is patterned by an etching process to define the future transistors areas. As a consequence, the **initial stress in the SiGe layer is relaxed at the edges** due to the introduction of **a free boundary condition** (Figure 3). Simulations of stress relaxation along the SiGe layer for different lengths have been performed. It appears that **for short areas (Lac<500nm), the side effects become predominant leading to partially relaxed film**. Simulations results have been **compared with experimental measurements** (Nano-Beam Diffraction) showing a reasonable agreement (Figure 4).

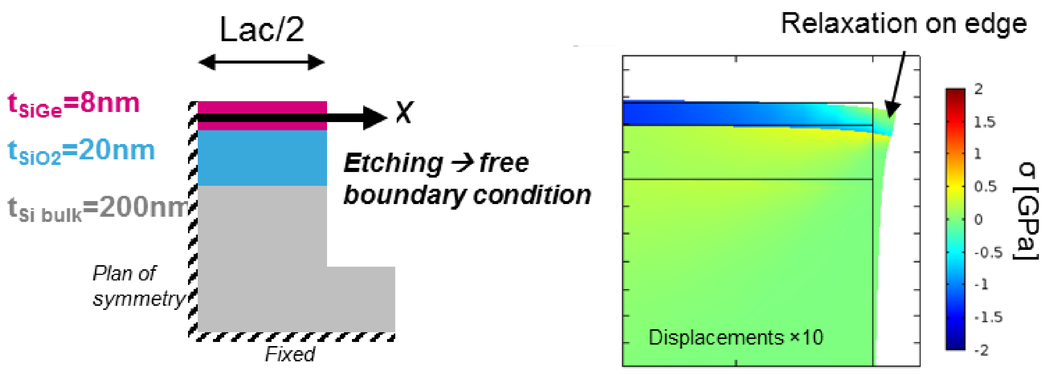

Figure 3: (left) schematic of the structure. (right) Stress mapping after relaxation on the edge.

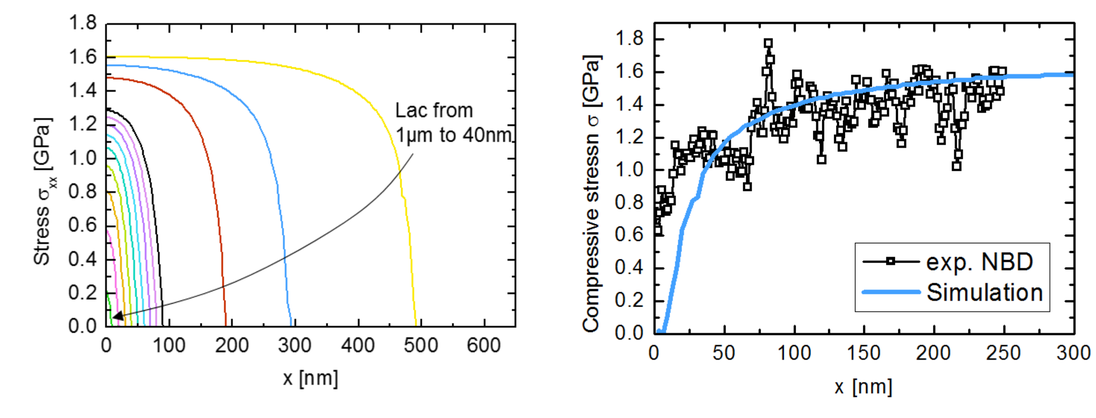

Figure 4: Stress according to the position along the SiGe film for different active lengths (left). Simulated stress profile from active edge compared with experimental results (NBD) (right).

2. Influence of Germanium concentrations

The FET with a $Si_{1-x}Ge_x$ channel being formed, **$Si_{1-y}Ge_y$ source and drain are deposited above the $Si_{1-x}Ge_x$ channel** aside from the gate (Figure 5). We studied the influence of Ge content both in the channel and in the source/drain on the final stress level in the area of interest, below the gate. We evidenced that **the stress induced by source and drain does not depend on the content of Ge in the channel** x_{Ge} but only on the device geometry and on the Ge content in the source/drain y_{Ge} (Figure 6). This result, highly counter-intuitive, evidences that 30% of Ge in source/drain on a 25% Ge active area is as efficient as on a 35% Ge one.

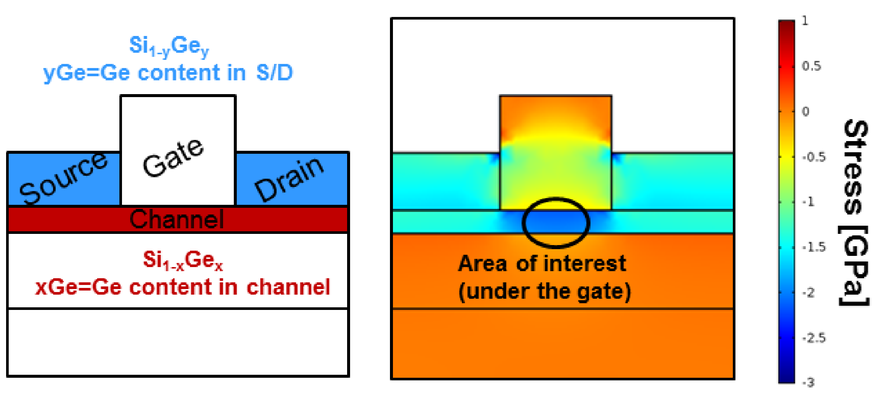

Figure 5: Illustration of the structure with Ge concentration in the channel xGe and in the Source/Drain yGe (left). Mapping of the final stress induced by SiGe in the channel and in the Source/Drain (right).

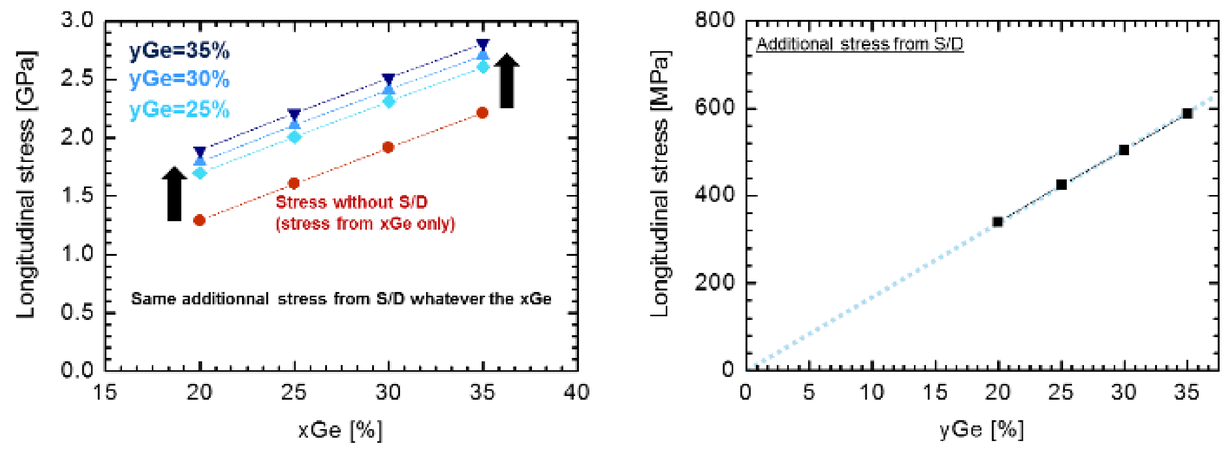

Figure 6: Stress under the gate as a function of Ge content in the channel xGe for different Ge content in Source/Drain yGe (left). The additional stress from S/D does not depend on Ge content in the channel. Stress under the gate as a function of Ge content in S/D showing a linear dependence (right).

Conclusion

The **integration of high level of stress** in field effect transistors is performed through incorporation of intrinsically strained SiGe layers. With the help of COMSOL simulations, we performed two studies addressing **the level of stress in the area of interest**. In the first case, we analyzed the **geometric effects of the SiGe film stress relaxation on the edges**. In a second time, we studied the final level of stress as a function of different Ge concentrations in both the channel and the source/drain. We found out that **the Ge content in the channel has no impact on the stress induced by the source/drain region**.

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