MODELING OF COMPLEX PHYSICS SPEEDS CHIP DEVELOPMENT

The symbiotic relationship between computer chips and computational modeling helps keep Moore's Law on pace at Lam Research Corporation.

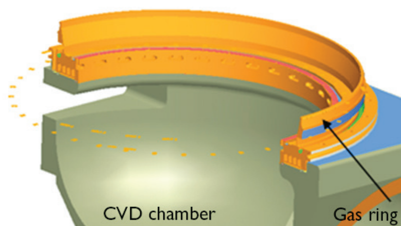
By **GARY DAGASTINE**

IN 1965, Gordon Moore predicted that ongoing technological advances would lead to a doubling of the number of transistors on computer chips about every two years, slashing the computing cost per calculation and exponentially increasing computing power.

But while more powerful chips are driving advances in computational modeling, the reverse is also true: Computational modeling is in turn driving progressively higher transistor densities and better architectures, reliability, and processing speeds. This virtuous circle is helping the semiconductor industry stay on pace with Moore's Law.

Lam Research Corporation is one of the world's leading suppliers of semiconductor manufacturing equipment and services. Its products are used to etch, deposit, and clean the ultrathin material layers from which semiconductors are built.

To meet the demands of the fast-paced semiconductor industry, Lam continually increases the performance, reliability, and availability of its products while also keeping their capital costs as low as possible. Many departments at Lam use computational modeling for the detailed analyses of nanoscale transistor features, to assess the performance of equipment, and for continuous product improvement



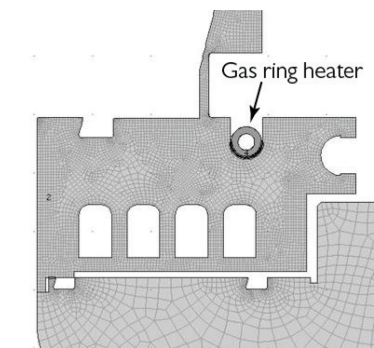


FIGURE 1: Gas is introduced into a chemical vapor deposition (CVD) chamber via a gas ring. The challenge is to keep the temperature of the ring uniform throughout the entire processing sequence.

involving many different scale levels.

The company's Computational Modeling and Reliability Group, headed by Peter Woytowitz, serves as a centralized internal resource for product research, development, and support. "Lam's goal is to be first to market with the best technology, but

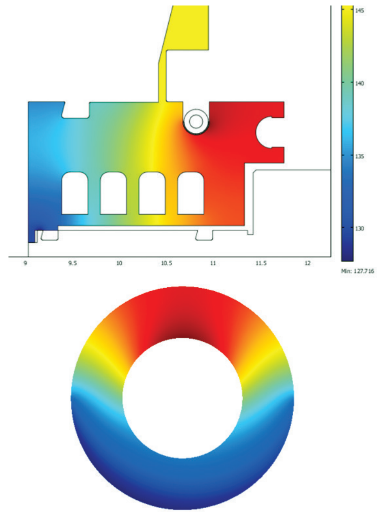


FIGURE 2: Lam is using the Heat Transfer Module in COMSOL Multiphysics® to help predict temperature uniformity under various operating conditions for CVD chamber gas ring heaters.

because our customers' processes and needs are constantly changing it's imperative for us to be fast and efficient. COMSOL Multiphysics helps us do that," he noted.

» SIMULATION LEADS TO BETTER CONTROL OF TEMPERATURE UNIFORMITY

IN SEMICONDUCTOR manufacturing, integrated circuits are fabricated on a wafer of semiconducting material. The circuits are built from multiple layers of different conducting and insulating materials that must follow an extremely precise design. These layers—some now only a few nanometers thick—are created via a series of many different processes that involve multiple aspects of material deposition, patterning, and selective removal.

Among the equipment used to deposit these layers, or thin films, of material onto a wafer are chemical vapor deposition (CVD) tools. A wafer is placed into a sealed CVD chamber for processing, and gas con-

taining the material to be deposited is introduced to the chamber. In one design, this is done via a gas ring that distributes the gas uniformly throughout the chamber (see Figure 1). The gas is energized to its plasma state to help drive the material onto the wafer and is then exhausted from the chamber.

It's imperative that the temperature of the gas ring be both uniform and hot enough throughout the entire process to minimize the amount of material deposited on it. If the desired temperature control is not achieved, then repeated thermal cycling can cause microscopic particles to break off the ring and fall onto a wafer, creating defects that could ruin the wafer. Particles are one of the leading causes of defects on otherwise good—and expensive—wafers in progress.

Using simulation, engineers design the heating and cooling channels within the gas ring, as well as an external heater to control gas ring temperature accurately during all phases of the CVD process. This entails both cooling the ring during plasma heating and heating it appropriately at other times (see Figure 2).

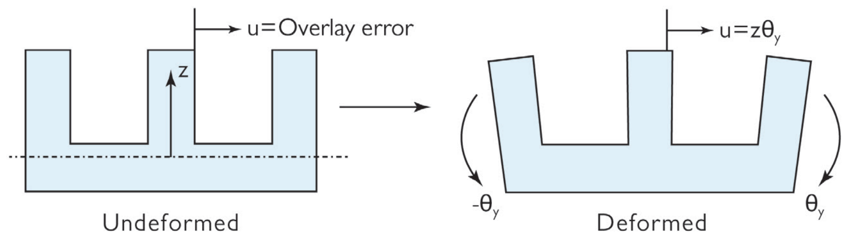


FIGURE 3: The cross-section at left shows an undeformed structure that introduces no photolithographic overlay error. On the right, a semiconductor wafer deformed by various stresses tilts, thereby introducing overlay error.

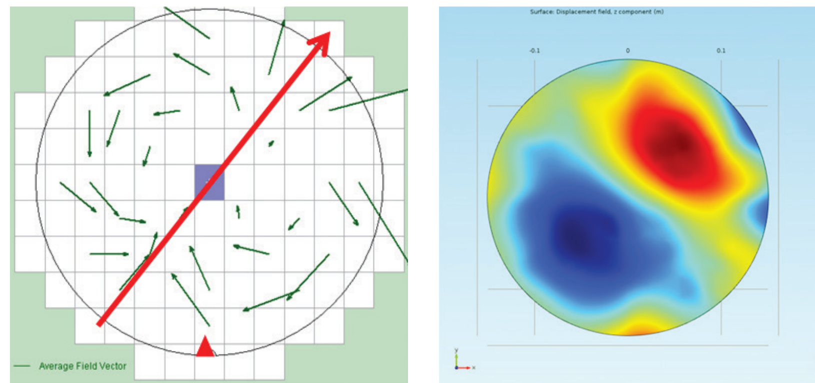


FIGURE 4: At left is a map of vectors contributing to wafer bow. The software resolved them into wafer displacement contour maps. On the right is a view in the x-y plane.

» MAJOR INSIGHTS GAINED INTO WAFER DEFORMATION IMPACTS

ANOTHER PROJECT at Lam was to study the effects of wafer deformations on photolithography, a key chip-manufacturing process similar to the process by which a photograph is developed on photosensitive paper.

During photolithography, light shines through a pattern known as a mask onto a photosensitive semiconductor wafer surface, and a layer of material is deposited onto and/or etched into the wafer according to the mask pattern. A series of masks are used to successively pattern layers until the integrated circuit is complete.

With the feature sizes on advanced chips now measuring 22 nanometers or less, many seemingly minor wafer distortions can have major deleterious effects on patterning accuracy. "Minute distortions of the wafer can cause misalignment and can distort features," describes Woytowitz. "This can then affect the ability of the photolithography process to accurately align and pattern the wafer."

Using COMSOL, analysts can identify any deviations from the desired pattern, called overlay error (see Figure 3), to determine if these defects were caused during the manufactur-

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> —PETER WOYTOWITZ, DIRECTOR OF ENGINEERING, LAM RESEARCH CORP.

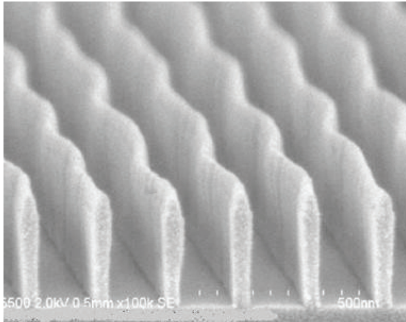


FIGURE 5: Photomicrograph showing the buckling of dummy structures used as building blocks to fabricate high aspect ratio interconnect for advanced computer chips.

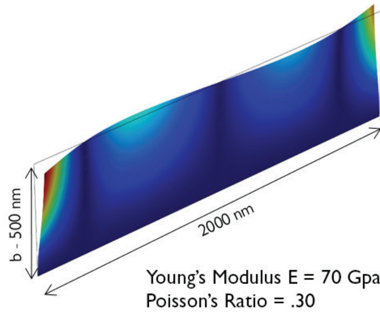


FIGURE 6: The Structural Mechanics Module in COMSOL Multiphysics can predict how buckling will occur in high aspect ratio chip interconnect.

ing process. If so, the performance of those tools can be optimized.

Woytowitz's group uses simulation to study how Lam's tools affect wafer deformation and then to determine if these deformations would impact photolithography. Plate theory, in conjunction with plate elements, is used to help characterize and correlate these distortions with measurable overlay errors.

For example, physical displacement from the horizontal plane, or wafer bow, is a significant contributor to overlay error. Before photolithographic processing, semiconductor wafers typically exhibit a bow of as much as 100 µm. Even when electrostatically bound to a tool's chuck for processing, or "clamped," they still may displace about 1 µm (see Figure 4).

Through simulation, Lam has determined that 1 µm of wafer bow generates overlay errors of about 10 nm. Since allowable overlay errors on today's advanced chips are generally about 10 nm (although they can be less), that is right at the allowable limit. Instead of a difficult and time-consuming trial-and-error testing process, simulation helped to quickly and precisely correlate the degree of wafer bow with overlay error.

» SUSCEPTIBILITY TO BUCKLING CAN NOW BE PREDICTED

THE USE OF high aspect ratio structures and features on today's chips is growing in order to save space, particularly for the metal lines known as interconnects that connect a chip's transistors.

The fabrication of interconnect is a multistep process. First, temporary lines are built from a film such as amorphous carbon by first depositing the material, then etching a series of closely spaced trenches into the film. Next, the trenches are filled with a dielectric (insulating) material, the temporary structures are etched away, and metal is deposited into the now-vacant spaces, forming tall, thin lines of metal interconnect.

However, manufacturers found that sometimes the temporary structures would buckle (see Figure 5). This buckling was not well understood, but if it could be predicted, then Lam could determine which high aspect ratio geometries would be successful in a production environment.

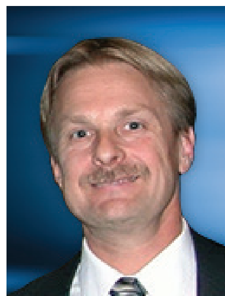
Woytowitz's group theorized that the buckling resulted from intrinsic compressive stress or possibly from mismatching coefficients of thermal expansion.

To investigate, they built COMSOL models, taking into account Young's modulus, for measuring the stiffness of an elastic material, and Poisson's ratio, the ratio of transverse to lateral strain. They compared these results with experimental values.

Analysis to date confirms that it is largely a buckling problem, and with an appropriate adjustment factor to correlate theory to experimental data, simulation can be used to predict when and how buckling will occur (see Figure 6).

» MODELING IS AN INCREASINGLY IMPORTANT TOOL

"**COMPUTATIONAL MODELING** is playing an increasingly important role at Lam, and we rely heavily on it," Woytowitz concludes. "COMSOL isn't the only tool we use, but its accuracy, ease of use, and the common look and feel of its user interface for many different physics domains allow us to become productive with it much more quickly and deeply than with other tools. These projects are just a few examples of how we are putting it to use." ◎



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Peter Woytowitz, Director of Engineering, Lam Research Corp.